

**IN THE SPECIFICATION:**

Kindly replace the paragraph beginning on page 2, line 11, with the following:

The present invention is related to the following commonly-assigned, copending applications:

“Multi-Mode Iterative Detector”, filed on April 27, 2000 and assigned application Serial No. 09/559186, the contents of which are incorporated herein by reference,

“LDPC Encoder and Method Thereof”, filed on even date and assigned application Serial No. 09/730,752 (Attorney Docket No. MP0064), the contents of which are incorporated herein by reference,

“LDPC Decoder and Method Thereof”, filed on even date and assigned application Serial No. 09/730,603 (Attorney Docket No. MP0065), the contents of which are incorporated herein by reference, and

“Address Generator for LDPC Encoder and Decoder and Method Thereof” filed on even date and assigned application Serial No. 09/730,597 (Attorney Docket No. MP0063), the contents of which are incorporated herein by reference.

Kindly replace the paragraph beginning at page 7, line 12, with the following:

According to a thirteenth aspect of the present invention, a code rate =  $(P_1 \cdot P_2 + P_1 - P_2 - P_3 + 2) / (P_1 \cdot P_2)$ .

Kindly replace the paragraph beginning at page 9, line 26, with the following:

Fig. 1A is a block diagram of a generalized data transmission system. The generalized data transmission system comprises a linear block code encoder 110, a communication channel 120 and a linear block code decoder 130. The operation of the generalized data transmission system will now be discussed. Input data is encoded by linear

block code encoder 110, which generates parity data in a known manner utilizing linear block codes. One example of a linear block code is a low-density parity-check (LDPC) which is discussed by Robert G. Gallager in *Low-Density Parity-Check Codes*, 1963, M.I.T. Press and by Zining Wu in *Coding and Iterative Detection For Magnetic Recording Channels*, 2000, Kluwer Academic Publishers, the contents of each of which are incorporated in their entirety by reference. The data is then transmitted over communication channel 120. The data from communication channel 120 is then decoded by linear block code decoder 130 in a known manner.

Kindly replace the paragraph beginning at page 10, line 29, with the following:

Transmitter 310 transmits the combined user and parity data from multiplexer 306 typically as an analog signal over communication channel 401 in the channel domain. Communication channel 401 may include any wireless, wire, optical and the like communication medium. Receiver 500 comprises an analog to digital converter 502 to convert the data transmitted on communication channel 401 to a digital signal. The digital signal is input to soft channel decoder 504, which provides probability information of the detected data. Soft channel decoder 504 may be implemented by a soft Viterbi detector or the like. The output of the soft channel decoder 504, which is in the channel domain, is converted into the linear block code domain by deinterleaver 510. Deinterleaver 510 is constructed similarly to deinterleaver 308. Soft linear block code decoder 506 utilizes this information and the parity bits to decode the received data. One output of soft linear block code decoder 506 is fed back to soft channel decoder 504 via interleaver 512, which converts data in the linear block code domain to the channel domain. Interleaver 512 is constructed to perform the reverse operations of deinterleaver 510. Soft channel decoder 504 and soft linear block code decoder 506 operate in an iterative manner to decode the detected data.

Kindly replace the paragraph beginning at page 11, line 16, with the following:

An alternative to incorporating deinterleaver 308 in transmission section 300 and deinterleavers deinterleaver 510 and 514 and interleaver interleavers 512 and 514 in receiving section 500 is to utilize utilize an address generator to provide an address of the appropriate equation of the linear block code encoder. The address generator is described in “Address Generator for LDPC Encoder and Decoder and Method Thereof” filed on even date and assigned application Serial No. 09/730,597 (Attorney Docket No. MP0063), the contents of which are incorporated herein by reference. As discussed therein the linear block code encoder is not dependent on a position of a bit interleaved. Rather the linear block code encoder only requires a list of equations for a given bit. In other words, there is no need to process the data in the order defined by the deinterleaver, instead data may be processed in the same order as it is written to the channel. This can be accomplished by incorporating an address generator to provide an address of the appropriate equation of the linear block code encoder. This principle can be similarly applied to the soft linear block decoder. As a result, and as illustrated in Fig. 2, deinterleaver 308 of the conventional system is now replaced by address generator 328, and deinterleaver 510 is now replaced by address generator 530. Accordingly, there is no requirement for the physical interleaving of data in the receiver 500’ illustrated in Fig. 2, since the data remains in the same order as the order of bits of data in the channel throughout this system. The order of bits of data transmitted through the channel is referred to as the channel domain.

Kindly replace the paragraph beginning at page 12, line 18, with the following:

The parity matrix can be generalized as comprising M tiers ( $M \geq 2$ ), each tier  $i$  comprising a row of identity matrixes  $I_{P_i}$  of rank  $P_i$ . The matrix is arranged such that  $P_1 < \dots < P_i < \dots < P_M$  and  $P_1, P_i, P_M$  are mutually prime. The number of columns in the preferred matrix is less than or equal to  $(P_1 \times P_2)$ . As can be readily seen, for tiers greater than 2, the last matrix in each row is not complete. Equation 8A is illustrative of a partial identity matrix of rank [[4]] 3.

Kindly replace the paragraph beginning at page 13, line 16, with the following:

For M=3, the matrix has a dimension of  $(P_1+P_2+P_3) \times (P_1 \cdot P_2)$ , ~~dmin~~ Dmin = 6 and tc = 3. The code rate for the matrix =  $(P_1 \cdot P_2 - P_1 - P_2 - P_3 + 2) / (P_1 \cdot P_2)$ .